A SINGLE-CHIP 1.9 GHz RF TRANSCEIVER MMIC USING GaAs MESFET TECHNOLOGY

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Abstract

This paper presents a newly developed single-chip RF transceiver MMIC for 1.9 GHz PHS wireless communications using a GaAs MESFET technology. The MMIC features a complete RF transceiver which includes an SPDT switch, a 2-stage LNA, a down-mixer, a double balanced up-mixer, an AGC amplifier and a 2-stage PA with an automatic gate-bias control circuit. The transceiver also features on-chip 50 Ω impedance matching, with a chip size of 9.3 mm^2 and packaged in a 48pin TQFP with heat sink.

Introduction

Since the introduction of the PHS, chip-set and single-chip solutions of the transceiver MMIC have been developed for reducing the size and the cost of handsets [1]−[4]. This paper reports an RF transceiver that has been successfully integrated onto a single chip fabricated in a GaAs MESFET process. Compared with the previous solutions, this chip has a higher integration level and features a complete RF transceiver developed for low cost 1.9 GHz PHS applications.

Transceiver Architecture

The block diagram of the transceiver chip is shown in Fig. 1. The receive chain of the transceiver includes a 2-stage LNA, a dual gate down-mixer, an LO buffer. The transmit chain includes LO and IF 1-to-2 baluns, LO buffers, a double balanced Gilbert up-mixer, a 2-to-1 balun, AGC circuits with active attenuation and a 2-stage PA with an automatic gate-bias control circuit. In addition, an SPDT switch to antenna and an LO driver to external LO PLL are also integrated onto the same chip. Careful partitioning of the transceiver MMIC makes it easy to test and accessible to each of the building blocks independently. Therefore the chip is flexible in configuration for either handset or base station application. The chip photo is shown in Fig. 2.

A low cost GaAs MESFET technology without substrate via holes is used. The process provides two types of DFETs: the deeper FETs with gate length = 1.0-μm and Vp = -2.1V for the PA and the shallower FETs with gate length = 0.5-μm and Vp = -0.9V for the rest of the circuits. All circuits use a regulated supply of 3V except for the PA which uses a -3.6V supply for gate bias and a raw 3.6 V supply for Vdd. The die size is 2.32 mm × 4.0 mm (or 9.28 mm^2). The package is a 48pin TQFP with heat sink.

Transceiver Circuits

The 2-stage LNA is designed in common source configuration. A complete on-chip input noise matching

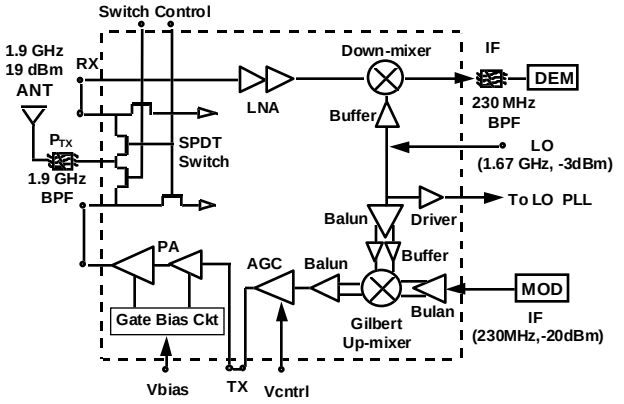

Fig. 1. The block diagram of 1.9 GHz RF transceiver MMIC for PHS applications.

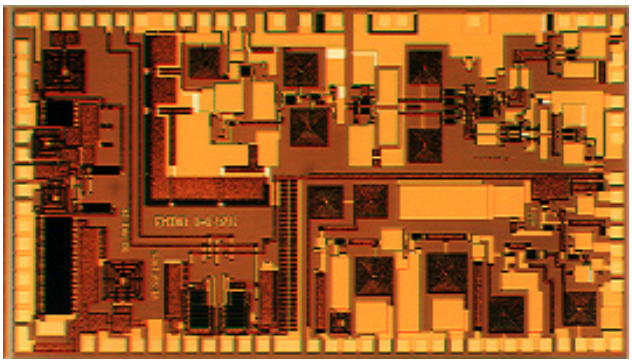

Fig. 2. The microphotos of the single-chip 1.9 GHz PHS transceiver MMIC.

gives a VSWR of 2.0. The overall receiver chain achieved a 3.4 dB noise figure, 22 dB conversion gain, 16 dB image attenuation and consumed 17.0 mA current.

The LO is splitted into 3 ways, one to the LO buffer for the down-mixing, one to the LO balun for up-mixing, and one to the driver for the external LO PLL. The driver uses an active load, delivering a fundamental level of -6 dBm and the second harmonic level of less than −20 dBc.

The transmit chain consists of the upconverter, the PA and the SPDT switch.

The up-mixer and the AGC in the transmit chain form the upconverter which was originally designed for PHS chip-set solution [5], and then re-designed as a building block for the single-chip transceiver [6]. The circuits have incorporated on-chip 50 Ω input/output matching. The LO and IF 1-to-2 baluns are designed in common gate and common source configuration while the 2-to-1 balun is designed in a common drain and common source configuration. A careful layout of Gilbert mixer has resulted in a repeatable LO suppression of better than -33 dBc. The on-chip matching circuits have attenuated the image levels to -28 dBc. The AGC is made of two stages of amplifiers with a series active attenuator in between, providing a 25 dB dynamic gain control. The linear gain control provides output power adjustment against process variations and power attenuation in communication. The up-converter's ACP (Adjacent Channel Power) is better than − 68 dBc at controlled gains ranging from -1 dB to 22 dB, exceeding PHS specification requirements. The performance of the upconverter demonstrated that there is no need for a band-pass filter between the PA and the AGC circuits.

The 2-stage PA features on-chip 50 Ω input and output matching and an automatic gate-bias control circuit which stabilises PA's operating point against process variations [7]. Other design issues are also fully discussed in [7]. The measurement shows the PA has achieved 20 dB gain. At 1 dB compress point of 21.5 dBm, the ACP is - 68 dBc with PAE of 22%.

A symmetrical conventional SPDT switch is used. The control voltage has a positive polarity. The switch has an insertion loss of 0.9 dB, isolation of 23 dB, ACP of -70 dBc at 21 dBm power level.

Simulation and Measurement

Layout simulation techniques and accurate package models [8] were used in the simulation of the distributed and package effects using MDS simulator. An in-house Symbolic Defined Device (SDD) model has been developed to overcome the problems associated with ROOT and EEFET3 models during AGC circuit simulations [6].

The measured parameters of each building block is summarised in Table 1. Fig. 3 through Fig. 8 show the performance of each individual block. Fig. 9 through Fig. 12 show the performance of the whole transmitter excluding the 1.9 GHz BPF: its image level is −34 dBc, LO level is − 40 dBc, spurious and harmonic levels are less than − 30 dBc, ACP is less than − 60 dBc at all controlled P_{TX} levels within 21 dB range.

Conclusions

A new GaAs single-chip RF transceiver MMIC for 1.9 GHz PHS application is presented. The MMIC features a complete RF transceiver with a higher integration level. The Measurement shows the chip meets very well PHS specification and design target.

Acknowledgment

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TABLE 1. MEASURED PARAMETERS OF THE PHS TRANSCEIVER MMIC

Receive Chain (LNA + Down-mixer)			Up-mixer + AGC		
@P_{LO}(1667 MHz)=-3dBm, P_{RF}(1908 MHz)=-40dBm, Vdd=3V			@P_{LO} (1677 MHz) =-3dBm, P_{IF} (230 MHz) =-20dBm, Vdd=3V		
PARAMETERS	**VALUES**	**UNIT**	**PARAMETERS**	**VALUES**	**UNIT**
RX Conversion Gain	22.5	dB	TX Conversion Gain	24.5	dB
Noise Figure	3.4	dB	P1dB	2.0	dBm
P1dB	-9	dBm	LO leakage to TX	-35	dBc
IP3 (input)	-21	dBm	Image band attenuation	-28	dBc
LO leakage to RX	-37	dBm	Spurious	<-37	dBc
Idd (Vdd=3 V)	17.0	mA	Harmonics	<-40	dBc
VSWR LO-input (1.66GHz)	1.9		Idd	41.0	mA
VSWR RX-input (1.9GHz)	2.0		TX level flatness (1895~1918 MHz)	< 0.27	dB
VSWR IF-output (240MHz)	1.4		Gain Control Range	25	dB
Image band (1.44 GHz) attenuation	16	dB	Control Voltage	0~3	V
			VSWR TX-out (1.9GHz)	1.6	
LO Driver to PLL			VSWR LO-in (1.67GHz)	2.1	
LO driver output level	-6.0	dBm	VSWR IF-in (230MHz)	1.4	
LO output harmonics	< -20	dBc	-/+ ACP (output level 2dBm)	-68 / -68	dBc
Idd (Vdd = 3 V)	4.0	mA	-/+ ACP (output level -21dBm)	-69 / -69	dBc
SPDT Switch			**Power Amplifier**		
PARAMETERS	**VALUES**	**UNIT**	**PARAMETERS**	**VALUES**	**UNIT**
Series FET Width	1400	μm	Drive stage FET width	1440	μm
Shunt FET width	600	μm	Final stage FET width	6120	μm
Insertion Loss TX→ATN @ 21dBm	0.9	dB	Total operating current	180	mA
Isolation TX→ANT @22dBm	23	dB	Power Added Efficiency	22	%
Insertion Loss ANT→RX	0.54	dB	Gain	20.0	dB
Isolation ANT→RX	22	dB	P1dB	21.6	dBm
VSWR ANT→RX	1.7		ACP @ 21.5 dBm	-68	dBc
VSWR TX→ANT	1.9		Harmonics	< - 40	dBc
P1dB TX→ANT	26	dBm	VSWR input	1.3	
ACP @21dBm	-70	dBc	VSWR output	2.4	

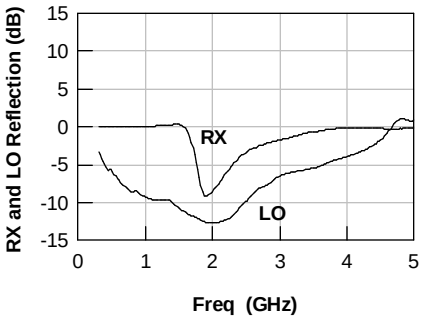

Fig. 3. Measured reflection coefficient of LO (1.66 GHz) and RX input (1.9 GHz).

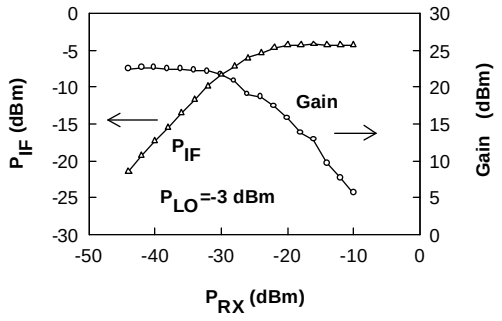

Fig. 4. Measured IF output power P_{IF} and conversion Gain of the receiver versus RX input power P_{RX}.

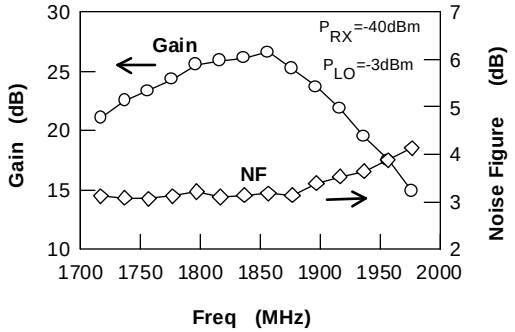

Fig. 5. Measured conversion gain and noise figure of the RF receiver versus band frequency.

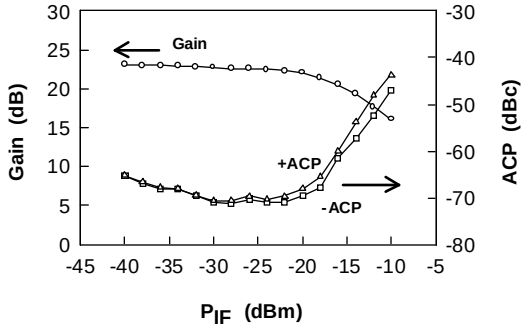

Fig. 6. Measured conversion gain and ACP versus IF input power P_{IF} for the upconverter.

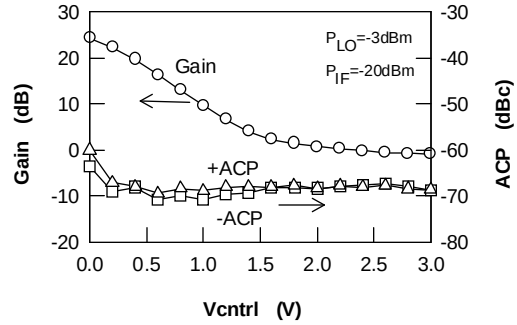

Fig. 7. Measured conversion gain and ACP versus AGC control voltage Vcntrl for the upconverter.

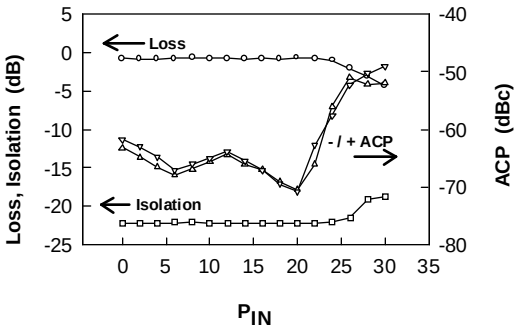

Fig. 8. Measured insertion Loss, Isolation and ACP versus input power P_{IN} for the SPDT switch.

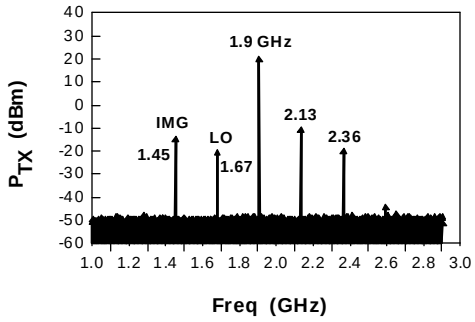

Fig. 9. Measured spectrum of output carrier power after SPDT switch without the 1.9 GHz band pass filter.

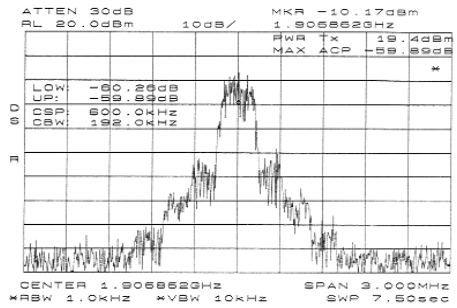

Fig. 10. Measured ACP of the whole transmitter (including the upconverter, the PA and the switch).

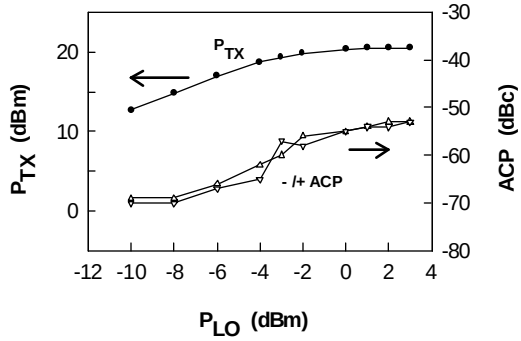

Fig. 11. Measured output carrier power P_{TX} and ACP of the whole transmitter versus LO input power P_{LO}.

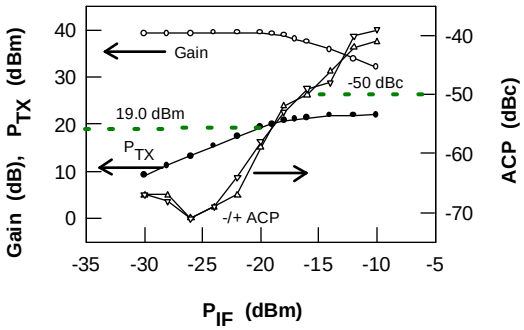

Fig. 12. Measured Gain, output carrier power P_{TX} and ACP versus input power P_{IN} for the whole transmitter.